

CLAIMS

What is claimed is:

1 1. A multi-channel segmented resistor string digital
2 to analog converter (DAC) comprising:
3 an A bit primary resistor string;
4 a plurality of buffer amplifiers, each buffering a
5 respective node between resistors of the primary resistor
6 string, outputs of the buffer amplifiers and ends of the
7 primary resistor string defining $2^A + 1$ primary string nodes;
8 a plurality M of B bit secondary resistor strings, the
9 nodes between resistors and ends of each secondary resistor
10 string defining $2^B + 1$ secondary string nodes; and,
11 a plurality of primary string switches coupled to each
12 primary string node, an output of each switch being coupled
13 to an end of a respective secondary resistor string.

1 2. The DAC of claim 1 wherein the offset voltage of
2 the buffer amplifiers is minimized by trimming.

1 3. The DAC of claim 1 further comprising M replica
2 current sources, each coupled to a respective secondary
3 resistor string, each replica current source providing a
4 current through the respective secondary resistor string to
5 cause a voltage across the respective secondary resistor

6 string equal to the voltage between adjacent primary string
7 nodes.

1 4. The DAC of claim 1 wherein the number of primary
2 string switches coupled to each primary string node is M,
3 outputs of the switches being coupled together in groups to
4 the ends of respective secondary resistor strings to
5 controllably couple the ends of each secondary resistor
6 string to any pair of adjacent primary resistor string nodes
7 using leapfrogging.

1 5. The DAC of claim 4 further comprising M replica
2 current sources, each coupleable to a respective secondary
3 resistor string with either polarity, each replica current
4 source providing a current through the respective secondary
5 resistor string to cause a voltage across the respective
6 secondary resistor string of a magnitude and a polarity equal
7 to the voltage between primary string nodes to which the
8 respective secondary resistor string may be coupled.

1 6. The DAC of claim 4 further comprised of:
2 M C bit tertiary resistor strings, nodes between
3 resistors of each tertiary resistor string and ends of each
4 tertiary resistor string defining $2^C + 1$ tertiary string
5 nodes; and,

6 a plurality of secondary string switches, each coupled
7 to a respective node of the secondary strings, each switch
8 being coupled to an end of a respective tertiary resistor
9 string.

1 7. The DAC of claim 6 wherein the resistance of each
2 resistor in the tertiary string is greater than the
3 resistance of each resistor in the secondary string.

1 8. The DAC of claim 6 further comprised of output
2 select switches coupled to the nodes of each tertiary
3 resistor string controllable to select the voltage on any one
4 node of each tertiary resistor string node as a DAC output
5 for a total of M DAC outputs.

1 9. The DAC of claim 6 wherein the number of secondary
2 string switches coupled to each secondary string node is M,
3 outputs of the secondary string switches being coupled
4 together in groups to the ends of respective tertiary
5 resistor strings to controllably couple the ends of each
6 tertiary resistor string to any pair of adjacent secondary
7 resistor string nodes using leapfrogging.

1 10. The DAC of claim 1 further comprised of:
2 M C bit tertiary resistors; and,

3 a plurality of secondary string switches associated with
4 the nodes of the secondary strings, each switch being coupled
5 to an end of a respective secondary resistor string.

1 11. The DAC of claim 10 wherein the number of secondary
2 string switches coupled to each secondary string node is M,
3 outputs of the secondary string switches being coupled
4 together in groups to the ends of respective tertiary
5 resistor strings to controllably couple the ends of each
6 tertiary resistor string to any pair of adjacent secondary
7 resistor string nodes using leapfrogging.

1 12. The DAC of claim 1 further comprising D bit
2 resistor strings in parallel with the primary resistor
3 string, where D is less than A, the D bit resistor strings
4 being laser trimmed.

1 13. A multi-channel segmented resistor string digital
2 to analog converter (DAC) comprising:
3 an A bit primary resistor string;
4 a plurality of buffer amplifiers, each buffering a
5 respective node between resistors of the primary resistor
6 string, outputs of the buffer amplifiers and ends of the
7 primary resistor string defining $2^A + 1$ primary string nodes;

8 a plurality M of B bit secondary resistor strings, the
9 nodes between resistors and ends of each secondary resistor
10 string defining $2^B + 1$ secondary string nodes;

11 a plurality of primary string switches coupled to each
12 primary string node, an output of each switch being coupled
13 to an end of a respective secondary resistor string;

14 a plurality M of C bit tertiary resistor strings, nodes
15 between resistors and ends of the tertiary resistor strings
16 defining $2^C + 1$ tertiary string nodes for each tertiary
17 resistor string;

18 a plurality of secondary string switches coupled to the
19 nodes of the secondary strings, each switch being coupled to
20 an end of a respective tertiary resistor string; and,

21 output select switches coupled to the nodes of each
22 tertiary resistor string controllable to select the voltage
23 on any one node of each tertiary resistor string node as a
24 DAC output for a total of M DAC outputs.

1 14. The DAC of claim 13 wherein the offset voltage of
2 the buffer amplifiers is minimized by trimming.

1 15. The DAC of claim 13 further comprising M replica
2 current sources, each coupled to a respective secondary
3 resistor string, each replica current source providing a
4 current through the respective secondary resistor string to
5 cause a voltage across the respective secondary resistor

6 string equal to the voltage between adjacent primary string
7 nodes.

1 16. The DAC of claim 15 further comprising D bit
2 resistor strings in parallel with the primary resistor
3 string, where D is less than A, the D bit resistor strings
4 being laser trimmed.

1 17. The DAC of claim 13 further comprising D bit
2 resistor strings in parallel with the primary resistor
3 string, where D is less than A, the D bit resistor strings
4 being laser trimmed.

1 18. The DAC of claim 13 wherein the number of primary
2 string switches coupled to each primary string node is M,
3 outputs of the switches being coupled together in groups to
4 the ends of respective secondary resistor strings to
5 controllably couple the ends of each secondary resistor
6 string to any pair of adjacent primary resistor string nodes
7 using leapfrogging.

1 19. The DAC of claim 18 further comprising M replica
2 current sources, each coupleable to a respective secondary
3 resistor string with either polarity, each replica current
4 source providing a current through the respective secondary
5 resistor string to cause a voltage across the respective

6 secondary resistor string of a magnitude and a polarity equal
7 to the voltage between primary string nodes to which the
8 respective secondary resistor string may be coupled.

1 20. The DAC of claim 13 wherein the resistance of each
2 resistor in the tertiary string is greater than the
3 resistance of each resistor in the secondary string.

1 21. The DAC of claim 20 wherein the number of secondary
2 string switches coupled to each secondary string node is M,
3 outputs of the secondary string switches being coupled
4 together in groups to the ends of respective tertiary
5 resistor strings to controllably couple the ends of each
6 tertiary resistor string to any pair of adjacent secondary
7 resistor string nodes using leapfrogging.

1 22. The DAC of claim 21 wherein the number of secondary
2 string switches coupled to each secondary string node is M,
3 outputs of the secondary string switches being coupled
4 together in groups to the ends of respective tertiary
5 resistor strings to controllably couple the ends of each
6 tertiary resistor string to any pair of adjacent secondary
7 resistor string nodes using leapfrogging.

1 23. The DAC of claim 13 wherein the multi-channel
2 segmented resistor string digital to analog converter is a
3 single integrated circuit.

1 24. A method of multiple channel digital to analog
2 conversion comprising:

3 providing an A bit primary resistor string;

4 providing M secondary resistor strings and M tertiary
5 resistor strings;

6 selectively coupling adjacent pairs of nodes in the
7 primary string to opposite ends of each secondary resistor
8 string;

9 selectively coupling adjacent pairs of nodes in each
10 secondary string to opposite ends of each tertiary resistor
11 string; and,

12 selectively coupling one node in each tertiary resistor
13 string, each as one output of the multiple channel digital to
14 analog conversion.

1 25. The method of claim 24 further comprising coupling
2 a D bit resistor string in parallel with the A bit resistor
3 string, where D is less than A, and laser trimming the D bit
4 resistor string.

1 26. The method of claim 25 further comprised of
2 coupling a current source in series with each secondary
3 resistor string, each current source providing a current
4 through the respective secondary resistor string equal to the
5 voltage difference between adjacent nodes in the first
6 resistor string.

1 27. The method of claim 26 wherein selectively coupling
2 adjacent pairs of nodes in the primary string to opposite
3 ends of each secondary resistor string is done using
4 leapfrogging, and wherein the polarity of the current sources
5 is varied accordingly.

1 28. The method of claim 27 wherein the resistance of
2 each resistor in the tertiary resistor string is selected to
3 be greater than the resistance of each resistor in the
4 secondary resistor string.

1 29. The method of claim 28 further comprised of
2 buffering the nodes between resistors in the primary resistor
3 string.

1 30. The method of claim 29 further comprised of
2 minimizing the offset voltage of the buffer amplifiers by
3 trimming.